ECE 2204: Electronics-I
VIRGINIA TECH
Course Syllabus (CRN *12175)*
Spring 2012 MWF 8:00-8:50am (Room: *ROB 105)*

I. ECE 2204 ELECTRONICS-I

Instructor: Prof. Mantu Hudait, Dept. of ECE, 626 Whittemore Hall
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Office Hours: Tuesday and Thursday: 1:30-2:30 and by appointment (e-mail please).

Prerequisites: ECE 2004 (C- or above). Co-requisite: ECE 2274

II. Course description

Introduction to basic electronic devices including diodes, field effect and bipolar transistors and their operating principles. Analysis of electronic circuits operating under DC bias and switching conditions. Application of devices in digital electronic circuits.

III. Major Measurable Learning Objectives:

Having successfully completed this course, the student will be able to:

1. Describe the operating principles of electronic devices including diodes and transistors.
2. Analyze electronic circuits operating under dc bias conditions.
3. Analyze electronic circuits operating under switching conditions.
4. Describe basic digital logic families.
5. Design and analyze simple digital gates.
6. Use PSpice to model circuits containing transistors and other electronic devices.

IV. TEXTS AND SPECIAL TEACHING AIDS

R.C. Jaeger and T. N. Blalock, Microelectronics Circuit Design, 4th Ed., McGraw-Hill.
J. G. Tront, **PSpice for Basic Circuit Analysis**, McGraw-Hill, 2007.
You can also download Pspice free from the site http://www.ece.vt.edu/ece3254/

V. COURSE OUTLINE

CONTENT	CHAPTER
Review of circuit analysis	Ch.1
Solid-state electronics	Ch. 2
Diodes and Diode circuits	Ch. 3
Field-effect transistors	Ch. 4
Bipolar junction transistors	Ch. 5
Digital electronics	Ch. 6
CMOS logic design	Ch. 7
Bipolar logic circuit	Ch. 9

V. Detailed Syllabus

ECE 2204	percentage
1. Introduction	5%
2. PN junction diode and diode characteristics	10%
3. Diode circuits and applications	10%
4. Bipolar junction transistor basics	5%
5. BJT characteristics	10%
6. BJT biasing and load line analysis	10%
7. MOS field effect transistor basics	10%
8. MOSFET biasing and DC analysis	10%
9. MOS logic design	10%
10. CMOS logic design	10%
11. BJT digital circuits	10%
Total	**100%**

VI. GRADING POLICY

Homework/other	20%
Exam I	20%
Exam II	20%
Final Exam	40%
	100%

Home Work

Homework problems will be typically be assigned on a weekly basis and will be due at the end of class one week following its assignment. Homework may be turned in one day late with a 25% deduction. **No assignments will be accepted beyond one day late,** except in the case of unforeseen, officially documented absences.

Each problem solution should be **neatly worked out**. If a given assignment requires multiple pages of work, it must be stapled together prior to submission. Use neatly trimmed 8.5" x 11" paper and write on one side only. When possible, sketch illustrative diagrams and label current, voltage, and other relevant quantities on the diagrams. Very rough sketches with no labels will receive no credit. Use industrially accepted notation for units, per discussion on Day 1 of class.

I will collect ALL assigned problems for grading. *However, all problems may not necessarily be graded*. I expect you to have worked ALL the problems and to be prepared to submit the problem solutions in the above format at the end of class on the date due.

You may consult with other students and with your instructor while you are working on assigned problems but your goal in consulting should be limited to exploring options and approaches rather than avoiding work. The ability to solve problems develops through disciplined effort and the exams will require you to be able to solve problems. To obtain full credit for a homework assignment you must submit it to your instructor in class on the due date.

In-Class Activities:

There will be regular activities assigned during class, which will require your participation and may result in a submission at the end of the class period. I will grade you on your preparation for these activities, your level of participation, and the conclusions that you draw from these activities. These activities should help strengthen your understanding of the course materials and assist in preparing you for the exams.

Exams:

There will be 3 mid-term exams and I will consider the best 2 score from your mid-term exam. No make-up exams will be given except for unforeseen, officially documented absences. If such a circumstance arises on a test date, it is your responsibility to contact me as soon as possible. If you expect to be absent on a test date for any legitimate reason (conferences, job interviews, project team competitions, etc.), it is your responsibility to give me sufficient prior notice so that we can make other arrangements. There will be a **FINAL exam** at the end of this course.

Academic Integrity:

The Virginia Tech Honor Code establishes the standard for **ACADEMIC INTEGRITY** in this course, and will be strictly enforced. *Discussion* of class material with your classmates or the instructor is encouraged; however, ALL submitted work, must represent your own efforts, and you must pledge to this effect on all work. For more details on the relevant honor codes, consult the websites listed below:

- Undergraduate Honor System, http://www.honorsystem.vt.edu/index.html

Announcements:

I will use Scholar to post homework assignments, homework solutions, and other information pertaining to the course materials. You should check your email and the Scholar on a regular basis. In case, I use any teaching materials not from the text book, I will post lecture notes in Scholar.

Attendance:

Attendance all lecture classes is expected and critical to your successfully completing the requirements of this course. While I may periodically check attendance against the class roll, I have no *explicit* penalties for your missing class. However, chronic absenteeism will be noted, and I will not be inclined to give such individuals the benefit of the doubt in judgment situations such as borderline final grades. In the event that you miss a lecture, it is your responsibility to ask one of your classmates or read text book. If you have a conflict with a scheduled exam or with the submission of any in-class assignments, you must make arrangements with your instructor well in advance so that alternate times can be scheduled.